

CLAIMS

1 1. A computer system, comprising:
2 a compiler receiving higher-level code and outputting lower-level code to enable a
3 processor to simultaneously process multiple multi-bit data elements in a single register, the
4 logic of the lower-level code including:
5 establishing at least first and second signed, multi-bit data elements in at least a first
6 register; and
7 simultaneously processing the elements.

1 2. The computer system of Claim 1, wherein the compiler accesses at least one of: a
2 compiler directive, a flag, or a configuration file, to decide when to make elements independent of
3 each other.

1 3. The computer system of Claim 1, wherein a first element is provided from a first data
2 set and a second element is provided from a second data set different than the first.

1 4. The computer system of Claim 1, wherein the compiler allocates a respective output
2 precision in a register for each data element to be processed in the register during a single cycle.

1 5. The computer system of Claim 1, wherein the compiler receives instructions not to
2 compile a predetermined portion of code received by the compiler.

1 6. The computer system of Claim 1, wherein an output precision or an input precision
2 is defined by means of a compiler directive, or a configuration file, or a variable definition.

3 7. A computer program device comprising:
4 a computer program storage device readable by a digital processing apparatus; and
5 a compiler program on the program storage device and including instructions executable by
6 the digital processing apparatus for performing method acts for outputting lower-level code to process
7 multi-bit, signed data elements, the lower-level code comprising:

8 computer readable code means for packing at least first and second data elements into
9 a single register; and

10 computer readable code means for processing the elements simultaneously.

1 8. The computer program device of Claim 7, further comprising:
2 flag means indicating whether a precision should be checked in at least one cycle.

1 9. The computer program device of Claim 7, further comprising:
2 compiler directive means for defining an input precision.

3 10. The computer program device of Claim 7, further comprising:

4 compiler directive means for defining multiple data sources of respective data elements
5 to be packed into a common register and operated on by an algorithm simultaneously with
6 each other.

1 11. A method, comprising:

2 defining at least one compiler directive, instructions, or configuration file for a
3 compiler defining at least one of:

4 an input precision for at least one data element; and

5 multiple data sources of respective data elements to be packed into a common register
6 and operated on by an algorithm simultaneously with each other.

1 12. The method of Claim 11, wherein the compiler determines first and second precisions
2 to be allocated in a single register to hold respective first and second signed data elements, and the
3 compiler generates a lower-level code from a higher level code to undertake method acts comprising:

4 packing the elements into the register; and

5 operating on the elements.

1 13. The method of Claim 12, wherein the register sends plural data elements
2 simultaneously to at least one computational subsystem.

1 14. The method of Claim 13, wherein the operation is a multiplication by a constant or
2 by a variable of known precision, or an addition, or a shift-left logical, or a subtraction, or a bitwise
3 AND, or a bitwise OR.

1 15. The method of Claim 14, wherein the elements are independent of each other as
2 defined by the compiler directive or configuration file.

1 16. The method of Claim 15, wherein the first element is provided from a first data set
2 and the second element is provided from a second data set different than the first.

1 17. The method of Claim 12, wherein the first element is a first partial element having
2 a related second partial element established in a second register, and the lower-level code causes the
3 first and second partial elements to be combined after processing.

1 18. The method of Claim 12, wherein the act of determining first and second precisions
2 includes determining the precisions such that the maximum negative number that can be represented
3 in an element is one larger than the maximum negative number that can be represented in the
4 respective precision.

1 19. The computer system of Claim 2, wherein the compiler generates instructions to pack
2 multiple data elements from respective data sources into a common register to be operated on by an
3 algorithm simultaneously with each other.

1 20. The computer system of Claim 19, wherein the first element is a first partial element
2 having a related second partial element established in a second register, and the lower-level code
3 output by the compiler causes the first and second partial elements to be combined after processing.

1 21. The method of Claim 11, wherein the compiler directive, instructions, or configuration
2 file embodies instructions to compile predetermined portions of code received by the compiler to be
3 executed simultaneously on packed data.

1 22. The computer program device of Claim 7, further comprising:
2 means for indicating whether a precision should be checked;
3 means responsive to the means for indicating for checking that the packed elements
4 do not overflow or underflow or achieve a maximum magnitude negative number
5 representable in the precision; and
6 means for, when packed elements overflow or underflow or achieve a maximum
7 magnitude negative number representable in the precision in a cycle, undertaking wrap or
8 saturation in the elements to prevent corruption of other data elements in a register, or
9 signalling an error to be handled by an error-handling routine in the program.

1 23. The computer system of Claim 4, wherein the compiler determines the output precision
2 based at least in part on an input precision.